Publications
Dr. Amit Kumar Pandey

Journal Papers:

1. A. Gupta, M. Rai, A. K. Pandey, S. Rai, D. Pandey, "A Novel Approach to Investigate Analog and Digital Circuit Applications of Silicon Junctionless-Double-Gate (JL-DG) MOSFETs", Silicon Springer. **Impact Factor: 2.67 (SCI, SCOPUS, UGC Care)**.
2. A. K. Pandey, T. K. Gupta, A. Gupta, and D. Pandey, "Keeper Effect on Nano Scale Silicon Domino Logic Transistors", Silicon Springer, pp **.** **Impact Factor: 2.67 (SCI, SCOPUS, UGC Care)**
3. V. Gupta, N. Kumar, H. Awasthi, S. Rai, A. K. Pandey, A. Gupta, "Temperature-dependent analytical modelling of graded-channel gate-all around (GC-GAA) junctionless field-effect transistors (JLFETSs)", Journal of Electronics Materials, Springer, vol. 50, pp. 3686-3691, 2021**.** **Impact Factor: 1.938 (SCI, SCOPUS, UGC Care)**
4. V. Gupta, H. Awasthi, N. Kumar, A. K. Pandey, A. Gupta, "A novel approach to model threshold voltage and subthreshold current of graded-doped junctionless-gate-all-around (GD-JL-JAA) MOSFETS", Silicon Springer, vol. 29, pp **.** **Impact Factor: 2.67 (SCI, SCOPUS, UGC Care)**
5. **S. Upadhyay, A. K. Pandey, and S. K. Pandey, "**Performance Evaluation of Low Power Adiabatic Techniques", TEXT Engineering and Management, vol.82, pp. 4132-4137, 2020**.** **(Scopus)**
6. S. Garg, T. K. Gupta, and A. K. Pandey, "A 1-bit full adder using CNFET based dual chirality high speed domino logic", International Journal Circuit theory and Applications, vol. 48, pp.115-133, 2020**.** **Impact Factor: 1.038 (SCI, SCOPUS)**
7. S. Garg, T. K. Gupta, and A. K. Pandey, "4:1 Multiplexer Using Dual Chirality CNTFET Based Domino Logic In Nano-Scale Technology", International Journal of

Electronics, vol. 107, no. 4, pp. 513-541, 2020**.** **Impact Factor : 0.939 (SCI, SCOPUS)**

8. A. K. Pandey, S. Upadhyay, T. K. Gupta, and P. K. Verma, "Low power, high speed and noise immune wide-OR footless domino circuit using keeper controlled method", Analog Integrated Circuits and Signal Processing, vol. 100, pp. 79-91, 2019. **Impact Factor: 1.337 (SCI, SCOPUS, UGC Care)**

9. A. K. Pandey, T. K. Gupta, and P. Verma, "Sleep signal controlled footless domino circuit for low leakage current", Circuit World, Emerald Publisher, vol.44, no. 2, pp. 87-98, 2018**.** **Impact Factor: 0.875 (SCI, SCOPUS).**

10. A. K. Pandey, P. Verma, R. Verma, and T. K. Gupta, " Analysis of noise immunity for wide OR footless domino circuits using keeper controlling network", Circuits Systems and Signal Processing, Springer, vol. 37, pp. 4599-4616, 2018. **Impact Factor: 2.225 (SCI, SCOPUS, UGC Care).**

11. T. K. Gupta, A. K. Pandey, and O. P. Meena, "Analysis and Design of Lector Based Dual-Vt Domino Logic with Reduced Leakage Current", Circuit World, Emerald Publisher, vol.43, pp.97-104, 2017. **Impact Factor: 0.875 (SCI, SCOPUS).**

12. A. K. Pandey, V. Mishra, R. A. Mishra, R. K. Nagaria, and V. K. Rao, "Conditional precharge dynamic buffer circuit", International Journal of Computer Applications, vol. 60, no. 6, pp.45-52, December 2012.

13. A. K. Pandey, R. A. Mishra, and R. K. Nagaria, "Low power dynamic buffer circuits", International Journal of VLSI Design & Communication Systems (VLSICS), vol. 3, no. 5, pp. 53-65, October 2012.

14. A. K. Pandey, R. A. Mishra, and R. K. Nagaria, "Leakage power analysis of domino XOR gate", ISRN Electronics, Hindawi, volume 2013, Article Id 271316, pp.1-7, January 2013.

15. A. K. Pandey, J. Tiwari, R. A. Mishra, R. K. Nagaria, and M. Tiwari, "Design of new low leakage power domino XOR circuit", International Journal of Computer Applications, vol. 65, no.1, pp.28-32, March 2013.

16. A. K. Pandey, R. A. Mishra, and R. K. Nagaria," Static switching dynamic buffer circuit", Journal of Engineering, Hindawi, volume 2013, Article Id 646214, pp.1-11, March 2013**.** **(SCOPUS, ESCI)**

17. A. K. Pandey, R. A. Mishra. and R. K. Nagaria, "Performance analysis of novel domino XNOR gate in sub 45n CMOS technology", WSEAS Transactions on Circuits and Systems, vol.12, no.2, pp. 48-57, February 2013. **(SCOPUS)**
18. A. K. Pandey, V. Mishra, R. A. Mishra, R. K. Nagaria, and V. K. Rao," Design of a trigger pulse operated low power domino circuit", The Mediterranean Journal of Electronics and Communication, vol.9, no.1, pp.485-493, January 2013. **(SCOPUS)**
19. A. K. Pandey, R. A. Mishra, and R. K. Nagaria, "New noise tolerant domino logic circuits", World applied sciences Journal, vol. 27, no.2, pp. 257-268, December 2013. **(SCOPUS)**
20. A. K. Pandey, R. A. Mishra, and R. K. Nagaria, "Leakage power analysis of dynamic footed circuits in 45nm CMOS Technologies", African Journal of Basic and applied sciences, vol.5, no.6, pp.268-275, 2013.
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International Conference

1. A. K. Pandey, R. A. Mishra, and R. K. Nagaria, "Low leakage power in sub-45nm with multiple threshold voltages and multiple gate-oxide thickness footed domino circuits", IEEE Conference, Nirma University, Ahmedabad, pp.1-6,08-10 December 2011.
2. P. Rani, A. K. Pandey, R. A. Mishra, and R. K. Nagaria, "A survey on different keeper design topologies for high speed wide AND-OR domino circuits", IEEE Student Conference, pp.1-4, 16-18 March, 2012.
3. A. K. Pandey, S. Kaur, R. A. Mishra, and R. K. Nagaria, "Leakage power reduction for domino circuits in 45 nm CMOS technologies", IEEE Conference (ICPCES), MNNIT Allahabad,17-19 December 2012.
4. S. Kumar, S. Singhal, A. K. Pandey, and R. K. Nagaria, "Design and simulation of low power dynamic logic circuit using footed diode domino logic", IEEE Student Conference, MNNIT Allahabad, pp.1-4, 2013.
5. Y. K. Mohan, A. K. Pandey, R. K. Singh, and R. K. Nagaria, "New domino logic designs for static outputs in evaluation phase for high frequency inputs", IEEE Student Conference, MNNIT Allahabad, pp.1-6, 2013.

National Conference

1. V. Kumar, A. K. Pandey, A. Gupta, and P. Giri, "Effect of hydrogen on flat band voltage of MOS Capacitor sensor", National Conference AMPDECS-2017, pp. 16-19, 29-31 March 2017.
2. P. Giri, M. Gupta, A. K. Pandey and V. Kumar, "Effect of thickness of buffer layer on the structural properties of ZnO thin films", hydrogen on flat band voltage of MOS Capacitor sensor", National Conference AMPDECS-2017, pp. 50-52, 29-31 March 2017.